We Claim:

1. A circuit for use in repairing memory arrays having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, said circuit comprising:

an analysis circuit for analyzing failures detected during testing of said memory array and for generating segment repair solutions for each segment;

said analysis circuit having registers for storing addresses of selected failures for each segment repair solution, said registers including row address registers for storing row addresses and one column address register for storing a column address;

said analysis circuit being operable to store row addresses and one column address in a unique order in segment repair solutions associated with the same segment; and

a segment repair solution processing circuit for identifying a best segment repair solution combination, consisting of one segment repair solution from each segment, having a number of different defective row addresses which is less than or equal to said predetermined number of spare rows, said best segment repair solution combination identifying rows and columns to be replaced by said spare rows and said spare column in each segment.

2. A circuit as defined in claim **1**, said row address registers corresponding in number to said predetermined number of spare rows.

3. A circuit as defined in claim **1**, wherein one or more segment repair solutions in the same or different segment share one or more row registers.

4. A circuit as defined in claim **3**, wherein row registers are shared between two or more segment repair solutions when said two or more segment repair solutions associated with different segments have the same repair strategy or when row registers associated with said segment repair solutions of the same segment would always store the same row address of a defective row.

5. A circuit as defined in claim **1**, each said register having an allocation register which is set when a valid address is stored in said each register.

6. A circuit as defined in claim **1**, said analysis circuit further including, for each segment repair solution, a status register for designating whether a status of a corresponding segment repair solution is non-repairable, repairable or no repair needed.

7. A circuit as defined in claim **1**, said analysis circuit including a plurality of segment repair engines for generating unique segment repair solutions associated with each segment, each said segment repair engine being logically identical and being operable to execute any of a predetermined number of different repair strategies and having associated defective row address registers and one defective column address register.

8. A circuit as defined in claim **7**, each said segment repair engine being responsive to a repair strategy parameter applied to said repair engines prior to initiating a memory test, said parameter indicating a number of spare rows to allocate before allocating the spare column of the segment.

9. A circuit as defined in claim **8**, wherein one or more repair engines of the same or different segments share one or more row registers.

10. A circuit as defined in claim **9**, wherein row registers are shared between two or more repair engines when two or more repair engines associated with different segments are assigned the same repair strategy parameter or when row registers in said two or more repair engines associated with the same segment would always store the same row address.

11. A circuit as defined in claim **8**, each said segment repair engine being operable to determine whether an initially defined repair strategy will not lead to a repair solution and to deviate to an alternative repair strategy when it determines that said initially defined repair strategy will not lead to a repair solution.

12. A circuit as defined in claim **8**, said plurality of segment repair engines associated with each segment is one more than said predetermined number of spare rows.

13. A circuit as defined in claim **11**, said alternative repair strategy comprising attempting to allocate a row register instead of a column register when multiple failures are detected in a word of said memory when attempting to allocate said spare column.

14. A circuit as defined in claim **8**, each said repair engine registers being configurable in serial mode for shifting the contents of said registers to said segment repair solution processing circuit and in hold mode for holding the contents of said registers constant.

15. A circuit as defined in claim **14**, said segment repair solution processing circuit further including a segment repair engine selection mechanism for selecting a segment repair engine and serially retrieving data stored in registers of a selected repair engine.

16. A circuit as defined in claim **15**, further including means for selectively forming a circular shift register of all registers associated with a repair engine, each said circular shift register having a serial input and a serial output, said serial output being connected to said serial input and to an input to said segment repair solution processing circuit.

17. A circuit as defined in claim **15**, further including means for selectively forming a first circular shift register consisting of all registers of all repair engines associated with a segment and for forming a second circular shift register consisting of registers of each of one repair engine of each segment, said second circular shift register having an output connected to said segment repair solution processing circuit.

18. A circuit as defined in claim **17**, said means for selectively forming including selector means associated with repair engines of each segment for receiving a serial output of the first circular shift register associated with said each segment and a serial output of a first circular shift register associated with another segment, each said selector means having an output connected to a serial input of its associated first circular shift register, each said selector means being responsive to a control signal for enabling said first circular shift registers or said second circular shift register.

19. A circuit as defined in claim **15**, further including means for selectively forming a circular shift register of all registers of each of one repair engine of each segment, said circular shift register having a serial input and a serial output, said serial output being connected to said serial input and to an input to said segment repair solution processing circuit.

20. A circuit as defined in claim **10**, wherein repair engines associated with different segments share at least one row register,

each said repair engine having an allocation register indicating whether a defective address stored in an associated shared row register has been allocated in its respective segment repair solution;

said segment repair solution processing circuit further including a segment repair engine selection mechanism for selecting one or more segment repair engines for retrieving data stored in the registers of said repair engines, said selection mechanism including:

means for forming a shared row register circular shift register having a serial output from a last of said shared row registers connected to a serial input of a first of said shared row registers and to an input of a selector controlled by a row select signal,

said selection mechanism including a second circular shift register consisting of other registers of said repair engines, said second circular shift register having a serial output connected to another input of said of said selector, said selector having an output connected to a serial input of said second circular shift register and to an input of said segment repair solution processing circuit.

21. A circuit as defined in claim **10**, further including for repair engines associated with different segments and sharing row registers, means defining a first path containing shared row registers and a second scan path containing all other registers of repair engines sharing said row registers, and selector means responsive to a control signal for connecting said first path or said second path to said segment repair solution processing circuit.

22. A circuit as defined in claim **10**, , further including, for repair engines associated with the same segment and sharing row registers, further including first selector means responsive to a repair engine select signal for selecting data stored in a first repair engine for transmission to said segment repair solution processing circuit and second selector means for selecting the contents of shared row registers of a second repair engine for transmission to said segment repair solution processing circuit.

23. A circuit as defined in claim **15**, said repair engine selection mechanism further including means for selectively forming a shift register of all registers of all repair engines of all segments, said shift register having a serial input and a serial output, said serial output being connected to said serial input and to an input to said segment repair solution processing circuit.

24. A circuit as defined in claim **8**, said segment repair solution processing circuit having a circuit for assembling all segment repair solutions combinations consisting of one repair engine selected from each segment; and a potential solution calculator for analyzing and rating each said segment repair solution combination.

25. A circuit as defined in claim **24**, said potential solution calculator having:

a set of working registers for receiving the contents of the registers of a selected repair engine;

a set of final solution registers for storing a solution having the best rating;

a selector responsive to a repair engine select signal for receiving a serial output of a selected repair engine; and

circuit means for evaluating a segment repair solution combination stored in said set of working registers; and

a circuit for performing potential solution operations using data loaded into said set of working registers and for storing a best solution in said set of final solution registers.

26. A circuit as defined in claim **8**, said segment repair solution processing circuit being operable, for different combinations of repair engines, to select a repair engine from each segment, read the repair information associated with the selected repair analysis circuits, calculate a repair solution using repair information read from selected repair analysis circuits, and assign a weight to a calculated memory repair solution; and store the memory repair solution having the highest weight.

27. A circuit as defined in claim **8**, said repair engine being configurable to execute a repair strategy independently of or cooperatively with other repair analysis circuits of the same or other segments.

28. A circuit for use in repairing a memory arrays having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, said circuit comprising:

at least one segment repair engine associated with each segment for analyzing failures detected during testing of a memory array and for generating a segment repair solution, each said repair engine having registers for storing addresses of selected failures, said registers including row address registers corresponding in number to said predetermined number of spare rows and one column address register;

said segment repair engines being logically identical and being operable to execute any of a predetermined number of different repair strategies and being responsive to a repair strategy parameter applied thereto prior to a memory test, said parameter indicating a number of row addresses to store before storing a column address of its associated segment; and

a segment repair solution processing circuit for identifying a best segment repair solution combination, consisting of one segment repair solution from each segment, having a number of different defective row addresses which is less than or equal to said predetermined number of spare rows, said combination identifying rows and columns to be replaced by said spare rows and said spare column in each segment.

29. A circuit as defined in claim **28**, further including:

each said row and column register including an allocation register indicating whether its associated row or column register contains a valid address;

each said repair engine further including a status register for classifying a segment repair solution as non-repairable, repair needed or no repair needed.

30. A circuit as defined in claim **29**, said segment repair solution processing circuit including:

a segment repair solution combination generating circuit for generating all possible segment repair solution combinations consisting of one segment repair solution selected from each segment; and

a circuit for analyzing and weighting each said combination, one segment repair solution at a time, said analyzing and weighting circuit:

assigning a lowest weight to a combination having a repair engine is designated non-repairable or to a combination having a repair engine requiring more spare rows than are available;

assigning a weight greater than a lowest value when a number of spare rows required by all segment repair solutions of a combination is less than or equal to said predetermined number of spare rows; and

comparing the weight of a combination against the weight of a best memory repair solution and storing the combination as a best memory repair solution if the weight of the combination is better than that of said memory repair solution.

31. A method of repairing a memory array having one or more memory segments each having one spare column and a predetermined number of spare rows common to all segments, said method comprising:

while testing the memory array for failures:

generating an equal number of unique segment repair solutions for each segment, each segment repair solution including one defective column address, if any, and a number of defective row addresses, if any, corresponding to said predetermined number of spare rows; and

after completing testing:

analyzing all combinations of segment repair solutions in which each combination includes one segment repair solution selected from each segment; and

identifying a best segment repair solution combination, consisting of one segment repair solution from each segment, having a number of different defective row addresses which is less than or equal to said predetermined number of spare rows, said best combination identifying rows and columns to be replaced by said spare rows and said spare column in each segment.

32. A method as defined in claim **31**, said generating unique segment repair solutions including storing a unique number of defective row addresses before storing a defective column address.

33. A method as defined in claim **31**, said generating a unique segment repair solution including, for a selected failure in an associated segment,

storing the row address of said selected failure when the number of previously stored row addresses is less than a number of row addresses unique to said segment repair solution;

otherwise, when the number of previously stored row addresses is greater than said unique number and a column address has not been previously stored, storing the column address of said selected failure;

otherwise, when a column address has been previously stored and the number of previously stored row addresses is less than said predetermined number of spare rows, storing the row address of said selected failure.

34. A method as defined in claim **33**, each said storing a row address and said storing a column address including setting a corresponding allocation bit indicating that a valid address has been stored.

35. A method as defined in claim **31**, said generating potential memory repair solutions including storing the defective column address of each segment repair solution in said combination and each of said same defective row addresses.

36. A method as defined in claim **31**, said determining which of the potential memory repair solutions provides the best solution including rating each potential memory repair solution according to predetermined criteria.

37. A method as defined in claim **33**, each said segment repair solution being identical except for the number of defective row addresses to store prior to storing a defective column address.

38. A method as defined in claim **33**, declaring a segment repair solution non-repairable when multiple failures have occurred in a word prior to storing a column address.

39. A method as defined in claim **33**, further including, declaring a segment repair solution non-repairable when a selected failure occurs after said number of defective row addresses have been stored, a defective column address has been stored and a number of defective row addresses corresponding to the predetermined number of spare rows have been stored.

40. A method as defined in claim **33**, further including, determining whether an initially defined segment repair strategy will not lead to a repair solution and deviating to an alternative repair strategy when it is determined that said initially defined repair strategy will not lead to a repair solution.

41. A method as defined in claim **40**, said alternative repair strategy comprising attempting to store a row address instead of a column address when multiple failures are detected in a word of said memory when attempting to store a column address.

42. A method of repairing a memory array having one or more memory segments, one spare column and a predetermined number of spare rows common to all segments, said method comprising:

while testing said memory array for failures:

generating an equal number of unique segment repair solutions for each segment, each segment repair solution including one defective column address, if any, and a number of defective row addresses, if any, corresponding to said predetermined number of spare rows, said generating segment repair solutions including storing a defective column address or defective row addresses in a unique order in which a unique number of defective row addresses are stored before storing a defective column address to a maximum of said number of row addresses and said column address; and

after completing said testing:

creating all segment repair solution combinations consisting of one segment repair solution selected from each segment;

generating potential memory repair solutions by determining which of the combinations contain compatible row addresses, storing the defective column address of each segment repair solution in said combination, and each of said compatible row addresses; and

rating each potential memory repair solution according to predetermined criteria to which of the potential memory repair solutions provides the best memory repair solution.

43. A method as defined in claim **42**, said generating a unique segment repair solution including, for a selected failure in an associated segment,

storing the row address of said selected failure when the number of previously stored row addresses is less than a number of row addresses unique to said segment repair solution;

otherwise, when the number of previously stored row addresses is greater than said unique number and a column address has not been previously stored, storing the column address of said selected failure;

otherwise, when a column address has been previously stored and the number of previously stored row addresses is less than said predetermined number of spare rows, storing the row address of said selected failure.

44. A method as defined in claim **42**, further including, prior to said performing said test, specifying for each said segment repair strategy of each said segment, a number of defective row addresses to store before storing the address of a defective column of the segment, and then storing a second number of additional defective row addresses corresponding to the difference between said predetermined number of spare rows and first number of defective row addresses.

45. A method as defined in claim **42**, said generating segment repairs solutions including assigning a status to each segment repair solution including a no repair needed status when a corresponding segment does not require repair, a repair needed status when the number of stored addresses is less than or equal to a predetermined number of addresses and a non-repairable status when the number of addresses which need to be stored is greater than said predetermined number of addresses.

46. A method as defined in claim **45**, said determining including considering only combinations which have a repair needed strategy status or a no repair needed status.